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Intel Legal Team
Intel Corporation
2111 NE 25th Avenue
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Date: December 18, 2005

TO:

Examiner: Board of Appeals c/o Chung, Phung M.
Art Unit: 2133
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FROM:

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APPLICATION INFORMATION:

Application No.: 09/746,676
Docket No.: P10141
Inventor: Miner, et al.
Filed: December 22, 2000
Assignee: Intel Corp.

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☑	Transmittal Form (SB/21)	1	pg(s)	☐	Drawings (____ figures)	0	pg(s)
☑	Fee Transmittal Form (SB/17)	1	pg(s)	☐	Petition for Extn' of Time (SB/22)	0	pg(s)
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TRANSMITTAL FORM

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Total Number of Pages in This Submission	35

Application Number	09/746,676
Filing Date	December 22, 2000
First Named Inventor	Miner
Art Unit	2133
Examiner Name	Chung, Phung M.
Attorney Docket Number	P10141

ENCLOSURES (*Check all that apply*)

- ☑ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
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- ☐ CD, Number of CD(s) _____
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- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☑ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Intel Corporation		
Signature			
Printed name	Justin B. Scout		
Date	Dec 18, 2005	Reg. No.	54,431

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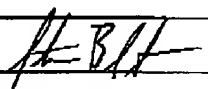
Signature			
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Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	09/746,676
Filing Date	December 22, 2000
First Named Inventor	Miner
Examiner Name	Chung, Phung M.
Art Unit	2133
Attorney Docket No.	P10141

METHOD OF PAYMENT (check all that apply)

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____ x	_____ =	_____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____ x	_____ =	_____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims Fee ($)	Multiple Dependent Claims Fee Paid ($)

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ / 50 =	_____ (round up to a whole number) x	_____ =	_____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): Brief in Support of Appeal	500.00

SUBMITTED BY

Signature	[signature]	Registration No. (Attorney/Agent) 54,431	Telephone 503-264-7002
Name (Print/Type)	Justin B. Scout		Date Dec 18, 2005

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Appl. No. 09/746,676 Attorney Docket: 042390.P10141

In The United States Patent and Trademark Office
Before The Board of Patent Appeals and Interferences

In re Patent Application of:	Miner, *et al.*	Examiner:	Chung, Phung M.
		Art Unit:	2133
Application No.:	09/746,676		
Filed:	December 22, 2000		
For:	TEST ACCESS PORT		

APPEAL BRIEF
IN SUPPORT OF APPELLANTS' APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Honorable Director of the United States Patent and Trademark Office
Washington, DC 20231

Sir/Madam:

Applicants (hereafter "Appellants") hereby submit this Brief in support of their Appeal from a final decision by the Examiner in the above-captioned case. Appellants respectfully request consideration of this Appeal by the Board of Patent Appeals and Interferences for allowance of the claims in the above-captioned patent application.

An oral hearing is not desired.

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TABLE OF CONTENTS

1. REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California 95052.

2. RELATED APPEALS AND INTERFERENCES

To the best of Appellants' knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision.

3. STATUS OF THE CLAIMS

Claims 1-37 are now pending in the above referenced patent application. Claims 1-37 were rejected for the third time in the Office Action mailed on June 16, 2005 and are the subject of this appeal.

4. STATUS OF THE AMENDMENTS

No amendments have been filed subject to the Final Rejection.

A copy of all claims on appeal is attached hereto as Appendix A.

5. SUMMARY OF THE CLAIMED SUBJECT MATTER

To provide a context for the invention, a Test Access Port (TAP) typically comprises a 4 or 5-pin serial test interface that is compliant with the IEEE 1149.1 specification. *IEEE Standard Test Access Port and Boundary-Scan Architecture*, IEEE Std 1149.1-1990. It may be used as an access mechanism to implement the boundary scan architecture, as well as other test modes typically employed to implement the Design For Testability (DFT) methodology on a given integrated circuit. Traditionally, microprocessor designs have employed a TAP as a mechanism for testing.

A TAP, in accordance with the IEEE 1149.1 specification, is employed by a large number of integrated chip designers and manufacturers. One of the purposes of a TAP is to facilitate testing of an integrated circuit. For example, a board manufacturer, attempting to verify that their board's components are properly coupled, may couple a number of the board's integrated chips' TAPS into a serial chain and shift data through that chain. This procedure is frequently referred to as 'boundary-scan', because data is scanned across the pin boundary of the board's integrated chips.

In another example, an integrated circuit designer may, as an example, wish to adjust the speed of the circuit's clock during specific logic stages. While the IEEE 1149.1 specification does not contain a specification regarding this form of testing, in order for the integrated circuit designer to accomplish this, one may, as one of many possible design choices, leverage the TAP specification to allow access to this test feature. Instructions substantially regulating the speed and timing of the clock may be scanned or shifted into the integrated circuit via the TAP. An integrated circuit designer may leverage a test access port that is substantially IEEE 1149.1

compliant to facilitate a variety of testing features, of which the above is merely one possible example.

The IEEE 1149.1 standard specifies a possible 4 pin interface which may be utilized to allow test instructions and associated test data to be fed into a component and, subsequently, may allow the results of execution of such instructions to be read out of the component. For testing features enumerated in the IEEE 1149.1 specification, information is communicated in a serial format. However, additional testing features that utilize a test access port, which is substantially IEEE 1149.1 compliant, may not be restricted in this fashion. (USPTO Publication 2002/0083387 A1, paragraphs 19-21.)

FIG. 5 is a diagram illustrating a distributed test access port mechanism implemented in a single-core processor. The Integrated TAP Controller (ITC) 510, which may include the TAPC and some data and control registers, may be coupled to distributed registers, such as, for example, 530, 531, & 532, and/or FUBs 521 & 522 via Integrated Test Bus (ITB) 550, for example. ITB 550 may comprise a grouping of data signals that allow the receiving registers and/or FUBs to locally generate control signals desired for operation, as opposed to generating the control signals directly from the TAPC. (USPTO Publication 2002/0083387 A1, paragraph 37.)

A technique for providing a improved IEEE 1149.1 compliant test access port for a multi-core processor may include: providing a TAPC on at least two processor cores, providing a TAP configuration register in the non-processor core, coupling the multiple core TAPCs and the non-processor core configuration register such that one of multiple routing and control configurations may be dynamically selected during operation. Such a device may reduce the number of pins employed on the IC package, and provide opportunities for reducing the number of testing

vectors and time utilized to test the multi-core device. In addition, such a device may allow a multi-core processor to be "plug-in" compatible with a single-core processor.

In light of the above illustrative context for the invention, it may be understood that FIG. 1 is a block diagram illustrating an embodiment of a multi-core processor in accordance with the invention. Embodiment 100 includes processor cores 110 & 120, although any number of processor cores may be used, and non-processor core 130, although any number of non-processor cores may be used. Both processor cores 110 & 120 may include TAPCs 111 & 121.

In the embodiment illustrated in FIG 1, both TAPCs may receive identical or substantially identical TLR, TMS, and TCLK signals via bus 150. However, the invention is not limited to embodiments where all TAPCs receive identical or substantially identical TLR, TMS and TCLK signals. The TAPCs may receive fully or partially independent TLR, TMS and TCLK signals. In addition, because the TLR signal is optional under the IEEE 1149.1 specification, some or all of the TAPCs may not receive the TLR signal. These fully or partially independent signals may each have fully or partially independent external IC pin interfaces or a particular routing technique may be used internally to the IC. For example, a routing scheme similar to that used in the embodiment illustrated in FIG 1 for the TDI and TDO signals, described below, may be employed in order to provide fully or partially independent TLR, TMS and TCLK signals. However, the invention is not limited to any particular routing scheme for these signals.

Both TAPCs 110 & 120 may produce their own TDO signals 113 & 123, which may be routed in accordance with one of many selectable configurations by TAP Control Switch 139. TAP Control Switch 139 provides a single TDO to external TDO signal 153. External TDI signal 152 may be routed in accordance with one of many selectable configurations by TAP

Control Switch 139. TAP Control Switch 139 provides TAPCs 111 & 121 with independent TDIs 112 & 122. TAP Control Switch 139 may route the TDI/TDO signals using multiplexer (MUX) or demultiplexer (DeMUX) components, however, one skilled in the art will instantly recognize that a variety of electrical components may be used to perform the desired routing operation.

TAP Control Switch 139 may be controlled by TAP Core Configuration Register 135. TAP Core Configuration Register 135 may be readable and writeable by, as taught by the IEEE 1149.1 specification, serially shifting data into and out of the register with the entering bit being TDI and the exiting bit being Register TDO 133. However, a variety of access mechanisms, either compliant or non- compliant with the IEEE 1149.1 specification, may be employed in order to read and/or write to Register 135. In this embodiment, TAP Core Configuration Control Logic 138 may receive ITBs 114 & 124, one from each TAPC. Alternately, in another possible embodiment, TAP Core Configuration Control Logic 138 may receive control signals that are more detailed and specialized than the generic signals employed in ITBs 114 & 124. MUX 136 may determine which processor core has control of non-processor core 130 and supplies TAP Core Configuration Control Logic 138 with the controlling ITB, ITB 134. Of course, any grouping of components, instead of MUX 136, may be used to perform the desired routing operation.

If multiple data and control registers are employed in the non-processor core, in accordance with the IEEE 1149.1 specification, each register will provide a TDO to the TAPCs. It may be desirable to reduce the number of TDOs returned to TAPCs 111 & 121 from the non-processor core. MUX 137 may be utilized to select which of the multiple TDOs is to be returned from non-processor core 130 to TAPCs 111 & 121. Of course, any grouping of components,

instead of MUX 137, may be used to perform the desired reduction operation. While the embodiment in FIG. 1 utilizes this TDO reduction the invention is not limited by supplying any particular number of TDO signals from non-processor core 130. The invention is also not limited to having only one non-processor core.

In the embodiment of the invention illustrated in FIG. 7, TAP Core Configuration Register 135 includes a bit to determine which processor-core's TAPC is allowed to control the non-processor core data and control registers, of which one is the TAP Core Configuration Register itself. Although the embodiment in FIG.1 illustrates two processor cores, the invention is not limited to embodiments with two processor cores. More bits may be used for embodiments with more than two processor cores. By default, this bit may be set to a substantially predetermined value. The substantially predetermined value may be loaded into the register upon a predetermined event such as, but not limited to: the IC receiving the "Power Good" signal from the power supply, activation of the IC's master reset pin, activation of the IC's TLR pin, or one or more of many other possible events. This bit may be used in conjunction with MUX 136 to determine which ITB the non-processor core will use as ITB 134.

In the embodiment of the invention illustrated in FIG. 7, TAP Core Configuration Register 135 includes a number of bits to determine the routing of the processor cores' TDI and TDO signals. Possible embodiments of routing configurations are illustrated in FIGs. 3 and 4. These routing configurations may be contrasted with the traditional routing configuration used for multiple processor systems, as illustrated by FIG. 2. In a multiple processor system two or more processors, each processor including a processor-core and a non-processor core, are utilized. In traditional multi-processor TAP routing, processors 210 & 220 may receive substantially identical TLR, TMS, and TCLK signals via bus 250. Processor 210 may receive its

TDI signal from the external TDI signal 252. Processor 210's TDO 212 may be daisy-chained via signal 260 to processor 220's TDI 223. Processor 220 then supplies its TDO signal to the external TDO signal 253. This allows one to shift data into either processor's TAPC. However the serial data chain, TDI 252 to TDO 253, is now effectively double that of a single processor's serial data chain. By doubling the effective length of a processor's serial data chain the amount of time to test the processor is effectively doubled.

In the embodiment of the invention illustrated in FIG.1, TAP Core Configuration Register 135 includes a number of bits to determine the routing of the processor cores' TDI and TDO signals. These bits may control which routing configuration of TAP Control Switch 139 is selected. One skilled in the art may realize a number of ways to implement the TAP Control Switch 139. For example, MUXs may be used, however the invention is certainly not limited to this embodiment of TAP Control Switch 139, and all are included within the scope of the present invention. Particular embodiments of these routing schemes are illustrated in FIGs 3 & 4. However, the invention is not limited to these illustrated routing schemes. The routing of external TDI 152 to external TDO 153 may involve routing the signals to the controlling TAPC's, as determined by TAP Core Configuration Register 135, the TDI/TDO signals. This may allow the multi-core processor to be accessed as if the controlling processor core existed within the IC. The non-controlling TAPC's TDI and TDO signals may be either disconnected or set to a substantially predetermined value. FIGs 3a & 3b illustrate embodiments where external TDI 152 and external TDO 153 are routed directly to the TDI and TDO signals of the controlling processor-core's TAPC. FIG 3a illustrates an example where processor-core 120's TAPC 111 is the controlling TAPC. FIG. 3b illustrates an example where processor-core 120's TAPC 121 is the controlling TAPC.

In the embodiments of the invention illustrated in FIGs 3c and FIG 3d, the ability to serially daisy-chain the processor-cores' TAPs is shown. TAP Core Configuration Register 135 may be used to control the order of the processor-cores in the serial daisy-chain. FIG. 3c illustrates a routing scheme where processor-core 110 may be first in the chain and processor-core 120 last in the chain. FIG. 3d illustrates a routing scheme where the order of the processor-cores in the serial chain is reversed from that illustrated in FIG. 3c. The order of the processor-cores in the daisy chain may be determined with the aid of the control bit found in TAP Core Configuration Register 135 or the order may be determined without reference to this bit.

In contrast to FIGs 3c & 3d, where the processor-core's serial data chains may be accessed in a serial fashion, FIG. 4 illustrates a possible routing configuration where the processor-core's serial data chains may be accessed in parallel. Once again, TAP Core Configuration Register 135 may control which of these routing configurations of TAP Control Switch 139 are selected. In this particular routing configuration, external TDI 152 is applied to the TDI signals of each processor-core's TAPC. If only one external TDO pin exists, the controlling TAPC's TDO signal may be placed on external TDO 153. FIG. 4a illustrates an embodiment where processor-core 110 is selected as the controlling TAPC and its TDO signal is placed on external TDO 153. FIG. 4b illustrates the case where processor-core 120 is selected as the controlling TAPC. (USPTO Publication 2002/0083387 A1, paragraphs 41-51.)

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The above referenced patent application has been reviewed in light of the Office Action, dated June 16, 2005, in which:

- claims 1-37 are rejected under 35 U.S.C. § 112, 2nd paragraph as indefinite;
- and claims 1-6, 8, 10, and 17 are rejected under 35 U.S.C. § 102(e) on Whetsel (US Patent No. 6,408,413 B1).

7. ARGUMENT

8. 35 U.S.C. § 112, 2nd paragraph

8.1. Claims 1-29: "Configuration"

The PTO has rejected claims 1-29 under 35 U.S.C. § 112, 2nd paragraph. This rejection is respectfully traversed.

Appellants begin with claim 1. Claim 1 recites:

> 1: (Previously Presented) An apparatus which comprises:
>
> a multi-core processor and
>
> at least one test control mechanism, including at least one test access port controller (TAPC) and a plurality of distributed data and control registers;
>
> said multi-core processor and said test control mechanism having a configuration so as to allow testing of said multi-core processor.

The PTO has claimed that "claim 1, line 5, 'configuration' is vague and indefinite." Appellants respectfully disagree.

Appellants respectfully note that the term "configuration" was not considered indefinite during the previous two Office Actions. However, Appellants also note that the PTO does have the right to bring a § 112 rejection against these claims at this stage.

8.1.1. Claim interpretation standard

MPEP § 2111 sets forth the standard for claim interpretation during examination.

> During patent examination, the pending claims must be "given the broadest reasonable interpretation consistent with the specification. ... The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach. *In re Cortright*, 165 F.3d 1353, 1359, 49 USPQ2d 1464, 1468 (Fed. Cir. 1999).

MPEP § 2111.01 further sets forth the standard of claim interpretation in both the case where a term is not defined in the specification and the case where the term is defined in the specification.

> When not defined by applicant in the specification, the words of a claim must be given their plain meaning. In other words, they must be read as they would be interpreted by those of ordinary skill in the art. *In re Sneed*, 710 F.2d 1544, 218 USPQ 385 (Fed. Cir. 1983)
>
> MPEP § 2111.01, 8th edition, 3rd paragraph.

> During examination, the claims must be interpreted as broadly as their terms reasonably allow. This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification. *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).
>
> MPEP § 2111.01, 8th edition, 1st paragraph.

MPEP § 2111 further sets forth that the Appellants may act has their own lexicographer, so long as the definition is not repugnant to the "plain meaning" of the defined term.

> Applicant may be his or her own lexicographer as long as the meaning assigned to the term is not repugnant to the term's well known usage. *In re Hill*, 161 F.2d 367, 73 USPQ 482 (CCPA 1947).

8.1.2. Claim interpretation as applied to Claim 1

Appellants respectfully assert that the Appellants use of the term "configuration" is within the plain meaning of the term and is therefore neither vague nor indefinite. Appellants start with the definition of "configuration":

> **configuration** (ken-fĭg'ye-rā'shen) noun
>
> 1. a. Arrangement of parts or elements.
>
> b. The form, as of a figure, determined by the arrangement of its parts or elements. *See synonyms at form.*
>
> 2. *Psychology.* Gestalt.
>
> 3. *Chemistry.* The structural arrangement of atoms in a compound or molecule.
>
> - config'ura'tionally adverb
>
> - config'ura'tive or config'ura'tional adjective
>
> The American Heritage® Dictionary of the English Language, Third Edition © 1996 by Houghton Mifflin Company.

Appellants select the most common definition of the term "configuration", definition 1. Appellants respectfully assert that this definition is within the scope established by M.P.E.P. § 2111.01. Appellants assert that since application does not deal with either Psychology or Chemistry, that definitions 2 & 3 are clearly unreasonable and outside the broadest reasonable interpretation of the term. Therefore, these definitions are outside the scope established by M.P.E.P. § 2111.01.

Appellants argue that definitions 1a and 1b are essentially synonymous. If they were not essentially synonymous, the American Heritage Dictionary would have made them definitions 1 & 2 and opposed to combining them into a single definition. However, for the sake of argument Appellants will illustrate that neither definitions 1a nor 1b are vague or indefinite.

The definition of the verb "arrange", from which noun "arrangement" derives (which is used in definitions 1a & 1b of "configuration"), may be enlightening and is:

> **arrange** (ə-rānj´) verb
>
> arranged, arranging, arranges verb, transitive
>
> 1.To put into a specific order or relation: dispose: arrange shoes in a neat row.
>
> 2.To plan or prepare for: arrange a picnic.
>
> 3.To bring about an agreement concerning; settle: *"It has been arranged for him by his family to marry a girl of his own class" (Edmund Wilson).*
>
> 4.*Music.* To reset (a composition) for other instruments or voices or for another style of performance.
>
> The American Heritage® Dictionary of the English Language, Third Edition © 1996 by Houghton Mifflin Company.

Once again, Appellants select the most common definition of the term "arrange", definition 1 "... a specific order or relation." Appellants respectfully assert that this definition is within the scope established by M.P.E.P. § 2111.01.

The definition of the noun "form" (which is used in definition 1b of "configuration") may be enlightening and is:

> **form** (fôrm) noun
>
> 1.a. The shape and structure of an object. b. The body or outward appearance of a person or an animal considered separately from the face or head; figure.
>
> 2.a. The essence of something. b. The mode in which a thing exists, acts, or manifests itself; kind: a form of animal life; a form of blackmail.
>
> 3.a. Procedure as determined or governed by regulation or custom. b. A fixed order of words or procedures, as for use in a ceremony; a formula.
>
> 4.A document with blanks for the insertion of details or information: insurance forms.
>
> ...
>
> 12. *Botany.* A subdivision of a variety usually differing in one trivial characteristic, such as flower color.
>
> The American Heritage® Dictionary of the English Language, Third Edition © 1996 by Houghton Mifflin Company.

Once again, Appellants select the most common definition of the term "form", definition 1a "the shape and structure of an object." Appellants respectfully assert that this definition is within the scope established by M.P.E.P. § 2111.01.

Therefore, Appellants respectfully assert that when Claim 1, lines 5 & 6 are read using the most common, plain meaning definition of the term "configuration" the lines would be understood to mean the following:

Original	said multi-core processor and said test control mechanism having a **configuration** so as to allow testing of said multi-core processor
Utilizing definition 1a	said multi-core processor and said test control mechanism **(*i.e.* the parts)** of having an **arrangement (*i.e.* put) in a specific order or relation** so as to allow testing of said multi-core processor.
Utilizing definition 1b	said multi-core processor and said test control mechanism **(*i.e.* the object)** having a **shape and structure** so as to allow testing of said multi-core processor.

Appellants assert that these three wordings of claim 1 are essentially synonymous and within the most common and plain meaning of the term "configuration." Therefore, one could

easily determine the meets and bounds of the claim without confusion. At worst, a casual reading of the specification and possibly a dictionary are all that is needed to fully understand the claim. Therefore, Appellants respectfully assert that the claim is neither vague nor indefinite and the rejection is improper. It is, therefore, respectfully requested that the rejection of this claim be withdrawn.

Claims 2-29 either depend from claim 1, or include a substantially similar and patentably distinct language as claim 1. It is, therefore, respectfully requested that the rejection of these claims also be withdrawn.

8.2. Claims 30-37: Claim 30, Lines 3 & 4

The PTO has rejected claim 30, and therefore claims 31-37, under 35 U.S.C. § 112, 2nd paragraph. This rejection is respectfully traversed.

Appellants begin with claim 30. Claim 30 recites:

30: (original) A method, comprising:
providing an indicator to identify a desired testing option;
based upon said desired testing option, dynamically routing signals between a plurality test access ports (TAPs);
wherein said plurality test access ports (TAPs) are part of a multi-core processor;
said multi-processor core including a plurality of processor cores.

Appellants respectfully note that these claims were not considered indefinite during the previous two Office Actions, and that the claims have not been amended. However, Appellants also note that the PTO does have the right to bring a § 112 rejection against these claims at this stage.

Appellants respectfully assert that claim 30 is neither indefinite nor fails to point out the claimed subject matter. While Figs. 3a, 3b, 3c, & 3d merely illustrate one non-limiting embodiment, they do illustrate an embodiment that helps explain the rejected claim.

As stated in the Office Action, the PTO is confused by the term "testing portion." Appellants respectfully point out that the claim cites the term "testing **option**" and that "testing **portion**" appears to be a slight inadvertent misreading of the claim. Fig 3 shows an embodiment with four possible testing options; it is understood that this merely illustrates one non-limiting embodiment. In Fig. 3a the option to select testing of only core #1 is illustrated. In Fig 3b the option to select testing of only core #2 is illustrated. Figs. 3c & 3d illustrate the options that test

the cores in series. As one would expect, which of these options is selected or desired is determined by a user.

The PTO asks "why dynamically routing signals between a plurality of test access ports (TAPs)?" Appellants respectfully note that a claim does not need to disclose the Appellants' motivations for making the invention; however, a few comments may further prosecution and understanding of the claim. As one possible reason, the signal may be dynamically routed in order to allow multiple testing options. If the signal's path was statically routed during manufacture, the user would have to select one testing option during manufacture. It may be important to remember that the term signal is not synonymous with the term physical wire. By dynamically routing the signal, a user may select a testing option on the fly. Once again Figs. 3a, 3b, 3c, & 3d illustrate an embodiment where the signals (TDI & TDO) are dynamically routed utilizing the Control Switch 139.

Appellants respectfully assert that claims 30-37 are neither indefinite nor fail to point out the claimed subject matter, especially when read in light of the specification and figures. It is respectfully requested that the foregoing claim rejections be withdrawn.

9. 35 U.S.C. § 102

9.1. Whetsel: Claims 1-6, 8, 10, and 17

The PTO has rejected claims 1-6, 8, 10, and 17 under 35 U.S.C. § 102(e) as being anticipated by Whetsel. This rejection by the PTO of these claims is respectfully traversed.

It is well-established that in order to establish a *prima facie* case of anticipation under § 102 of the patent statute, the PTO must provide a single prior art document that alone has every element and every limitation of the claim being rejected. Therefore, if even a single element or limitation is not met by the asserted document, then the PTO has not succeeded in establishing a prima facie case.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Appellants begin with claim 1. Claim 1 recites:

1: (Previously Presented) An apparatus which comprises:
a multi-core processor and
at least one test control mechanism, including at least one test access port controller (TAPC) and a plurality of distributed data and control registers;
said multi-core processor and said test control mechanism having a configuration so as to allow testing of said multi-core processor.

It is respectfully asserted that, as just one example of how the text cited by the PTO fails to meet the language of the rejected claims, Whetsel does not show, teach, use, or describe a plurality of **distributed data and control registers**. While Whetsel does show a plurality of TAPs, no TAP includes a plurality of **distributed data and control registers.** See, Whetsel Fig

17. Also, see Whetsel, Fig. 1 in which two data registers (boundary-scan and bypass) are shown, and no control registers are illustrated. It is noted that one skilled in the art of TAP design will understand that both a boundary-scan chain and a bypass register are considered, and referred to in the IEEE 1149 specification as data registers. See *IEEE Standard Test Access Port and Boundary-Scan Architecture*, IEEE Std 1149.1-1990, Chapters 9 & 10.

In summation, it is respectfully asserted that Whetsel (1) does not show distributed registers, and (2) does not show control registers. Appellants respectfully contend that Whetsel fails to satisfy a *prima facie* case of anticipation as directed by 35 U.S.C. § 102.

Claims 2-37 either depend from claim 1, or include a substantially similar and patentably distinct limitation as claim 1. It is, therefore, respectfully requested that the rejection of these claims also be withdrawn.

10. CONCLUSION

In view of the foregoing, it is respectfully asserted that all claims pending in this application, as amended, are in condition for allowance. If the Examiner has any questions, they are invited to contact the undersigned at 503-264-7002. Reconsideration of this patent application and early allowance of all claims is respectfully requested.

Respectfully submitted,

Dated: Sun. Dec 18, 2005

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APPENDIX A: CLAIMS APPENDIX

1: (Previously Presented) An apparatus which comprises:

a multi-core processor and

at least one test control mechanism, including at least one test access port controller (TAPC) and a plurality of distributed data and control registers;

said multi-core processor and said test control mechanism having a configuration so as to allow testing of said multi-core processor.

2: (original) The apparatus of claim 1, wherein said multi-core processor comprises at least two processor cores and at least one circuit comprising non-processor core logic.

3: (original) The apparatus of claim 2, wherein said multi-core processor and said test control mechanism having a configuration so as to allow testing of at least two processor cores of said multi-core processor.

4: (Previously Presented) The apparatus of claim 2, wherein said plurality of distributed data and control registers are located both within said at least two processor cores and within said at least one circuit comprising non-core logic.

5: (original) The apparatus of claim 4, wherein said at least one test control mechanism is substantially compliant with the IEEE 1149.1 specification.

6: (original) The apparatus of claim 4, wherein said at least one test access port controller (TAPC) is located within said at least two processor cores.

7: (original) The apparatus of claim 4, wherein said at least one test access port controller (TAPC) and at least one of said plurality of distributed data and control registers are coupled via an Integrated Test Bus (ITB).

8: (original) The apparatus of claim 4, wherein said distributed test control mechanism is controllable, at least in part, by one of said at least one test access port controller (TAPC).

9: (Previously Presented) The apparatus of claim 8, wherein which one of said at least one test access port controllers (TAPCs) controls said distributed test control mechanism is dynamically selectable during operation.

10: (original) The apparatus of claim 2, wherein at least one of the said at least two processor cores comprises one test access port (TAP) which includes one test access port controller (TAPC), and a plurality of distributed data and control registers.

11: (original) The apparatus of claim 10, wherein said test control mechanism and said at least two processor cores are coupled so as to provide multiple coupling arrangements, said multiple coupling arrangements being dynamically selectable during operation.

12: (original) The apparatus of claim 11, wherein said multiple coupling arrangements are selected from a group consisting essentially of coupling said test access ports substantially in series, coupling said test access ports substantially in parallel and coupling said test access ports for substantially independent operation.

13: (original) The apparatus of claim 10, wherein said at least one test control mechanism is arranged to allow at least one of said at least two processor cores' said one test access port (TAP) to be externally visible from said multi-core processor.

14: (original) The apparatus of claim 13, wherein said at least one test control mechanism is arranged to allow only one of said at least two processor cores' said one test access port (TAP) to be externally visible from said multi-core processor.

15: (original) The apparatus of claim 13, wherein said at least one test control mechanism is arranged to allow the selection of which at least one of said at least two processor cores' said one test access port (TAP) is externally visible from said multi-core processor to occur dynamically.

16: (original) The apparatus of claim 10, wherein said at least one test control mechanism is coupled to produce during operation an error signal if the output signals of said at least two processor cores' said one test access port (TAP) are not substantially equivalent.

17: (original) The apparatus of claim 2, wherein said at least one test control mechanism, said at least one processor core and said at least one circuit comprising non-processor core logic are

further coupled so as to allow testing of said at least one circuit comprising non-processor core logic.

18: (Previously Presented) A system which comprises:

a computing platform, including:

a memory to store instructions;

a multi-core processor to process instructions which includes:

a plurality of processor cores;

at least one circuit comprising non-processor core logic and

a test control mechanism, including at least one test access port controller (TAPC) and a plurality of distributed data and control registers;

said multi-core processor and said test control mechanism having a configuration so as to allow testing of said plurality of processor cores.

19: (Previously Presented) The system of claim 18, wherein said multi-core processor and said test control mechanism are capable of allowing testing of said at least one circuit comprising non-processor core logic.

20: (Previously Presented) The system of claim 18, wherein said plurality of distributed data and control registers are located both within said plurality of processor cores and within said at least one circuit comprising non-core logic.

21: (original) The system of claim 20, wherein said at least one test control mechanism is substantially compliant with the IEEE 1149.1 specification.

22: (original) The system of claim 20, wherein said at least one test access port controller (TAPC) is located within said plurality of two processor cores.

23: (original) The system of claim 20, wherein said at least one test access port controller (TAPC) and at least one of said a plurality of distributed data and control registers are coupled via an Integrated Test Bus (ITB).

24: (original) The system of claim 20, wherein said distributed test control mechanism is controlled, at least in part, by one of said at least one test access port controller (TAPC).

25: (Previously Presented) The system of claim 24, wherein which one of said at least one test access port controllers (TAPCs) controls said distributed test control mechanism is be dynamically selected during operation.

26: (original) The system of claim 18, wherein each of the said at least two processor cores comprises one test access port (TAP) which includes one test access port controller (TAPC), and a plurality of distributed data and control registers.

27: (original) The system of claim 26, wherein said test control mechanism and said at least two processor cores are coupled so as to provide multiple coupling arrangements, said multiple coupling arrangements being dynamically selected during operation.

28: (original) The system of claim 27, wherein said multiple coupling configurations are selected from a group consisting essentially of coupling said test access ports substantially in series, coupling said test access ports substantially in parallel, and coupling said test access ports for substantially independent operation.

29: (original) The system of claim 26, wherein said test control mechanism is coupled to produce, during operation, a signal that indicates whether the output signals of said at least two processor cores' said one test access port (TAP) are equivalent or substantially equivalent.

30: (original) A method, comprising:

providing an indicator to identify a desired testing option;

based upon said desired testing option, dynamically routing signals between a plurality test access ports (TAPs);

wherein said plurality test access ports (TAPs) are part of a multi-core processor; said multi-processor core including a plurality of processor cores.

31: (original) The method of claim 30, wherein the routing of said signals is selected from a group consisting essentially of coupling said test access ports substantially in series, coupling

said test access ports substantially in parallel, and coupling said test access ports for substantially independent operation.

32: (original) The method of claim 31, wherein providing an indicator to identify a desired testing option comprises storing control information in a register.

33: (original) The method of claim 32, wherein storing control information in a register comprises shifting said data into the register in a serial fashion.

34: (original) The method of claim 32, wherein storing control information in a register comprises a step in compliance with the operation of test data registers as described in the IEEE 1149.1 specification.

35: (original) The method of claim 30, wherein dynamically routing signals between a plurality of test access ports (TAPs) comprises dynamically routing signals between a plurality of test access port controllers (TAPCs) and a plurality of distributed data and control registers.

36: (original) The method of claim 30, wherein dynamically routing signals between a plurality of test access ports (TAPs) comprises only altering the routing of signals external to said plurality of processor cores.

37: (original) The method of claim 30, which further comprises producing a signal that indicates whether the output signals of said at least two processor cores' said one test access port (TAP) are equivalent or substantially equivalent.

APPENDIX B: EVIDENCE APPENDIX

To the best of Appellants' knowledge, there is no evidence submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132 or of any other evidence entered by the examiner and relied upon by appellant in the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision.

Appellants note that a series of declarations under 37 C.F.R. § 1.131 were made by the inventors and drafting attorney to establish a date of conception no later than June 5, 2000. This date is earlier than the effective date of the Swamy reference (U.S. Patent No. 6,686,759 B1, November 28, 2000) which was cited in a previous Office Action. That reference is no longer cited by the PTO. Therefore the § 1.131 declarations are not directly relied upon by appellant in the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision. These unnecessary pieces of evidence are not submitted.

APPENDIX C: RELATED PROCEEDINGS APPENDIX

To the best of Appellants' knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision.